Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **Q1**
2. **N. Q1**
3. **CLOCK 1**
4. **RESET 1**
5. **D1**
6. **SET 1**
7. **VSS**
8. **SET 2**
9. **D2**
10. **RESET 2**
11. **CLOCK 2**
12. **N. Q2**
13. **Q2**
14. **VDD**

**.055”**

**.059”**

**12 11 10 9**

**13**

**14**

**1**

**8**

**7**

**6**

**2 3 4 5**

**MASK**

**REF**

**4013**

****

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .04”**

**Backside Potential: VDD or FLOAT**

**Mask Ref: 4013**

**APPROVED BY: DK DIE SIZE .055” X .059” DATE: 8/17/21**

**MFG: SILICON SUPPLY THICKNESS .014” P/N: CD4013B**

**DG 10.1.2**

#### Rev B, 7/19/02